



TRANSMITTAL LETTER FOR RESPONSE

Attorney Docket No. 1003-0610

In re patent application of: Newell E. Chiesl

Serial No. 09/960,441

Filing Date: September 21, 2001

Examiner: Allan R. Wilson

Group Art Unit: 2815

For: Arrangement for Measuring Pressure on a Semiconductor Wafer and an

Associated Method for Fabricating a Semiconductor Wafer

TO THE COMMISSIONER OF PATENTS AND TRADEMARKS:

Transmitted herewith is a Response in the above-identified patent application. The fee has been calculated as shown below.

| CLAIMS AS AMENDED | | | | |
|-------------------------------|-------------------------------------|-------------------------|--------------------|--------------|
| | Claims Remaining After Amendment | Highest No. Paid For | Fee Calculation | Addit Fee |
| Total Claims | 20 | 20 | 0 X 18 | \$ 0 |
| Independent Claims | 3 | 3 | 0 X 84 | \$ 0 |
| Total Additional Fee Required | | | | \$ 0 |

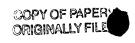
* Please provide any extensions of time which may be necessary and charge any fee which may be due to Deposit Account No. 13-0014, but not to include any payment of issue fees.

Respectfully submitted,

Harold C. Moore Attorney for Applicants Registration No. 37,892

August 19, 2002 Maginot, Moore & Bowman Bank One Tower/Center 111 Monument Circle, Suite 3000 Indianapolis, Indiana 46204-5115 (317) 638-2922





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Assistant Commissioner of Patents Washington, D.C. 20231

> I hereby certify that this correspondence is being ro deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner of Patents and Trademarks,

Washington, D.C. 20231 on August 19, 2002

(Date of Deposit)

Harold C. Moore

Name of person-mailing Document or Fee

Signature

August 19, 2002

Date of Signature

Re:

Application of:

Newell E. Chies

Serial No.:

09/960,441

Confirmation No.:

5776

Filed:

September 21, 2001

For:

Arrangement for Measuring Pressure on a Semiconductor Water and an Associated

Method for Fabricating a Semiconductor

Wafer

Group Art Unit:

2815

Examiner:

A. Wilson

Our Docket No.:

1003-0610

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the Restriction Requirement dated July 17, 2002 for the aboveidentified patent application, please consider the following election.